IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Wendell P. Noble et al.   Examiner: Michael Trinh

Serial No.:   09/551,027   Group Art Unit: 2822

Filed: April 17, 2000   Docket: 303.379US2

Title: CIRCUIT AND METHOD FOR A FOLDED BIT LINE MEMORY CELL
WITH VERTICAL TRANSISTOR AND TRENCH CAPACITOR

AMENDMENT AND RESPONSE

Commissioner for Patents
Washington, D.C. 20231

Applicant has carefully reviewed the Office Action mailed December 21, 2000. Detailed comments to the Office Action are found in the Remarks section below. Amendments to the specification and claims are found in the following Amendments section.

IN THE SPECIFICATION

Please replace the identified pages of the specification with the replacement page as provided in the enclosed Clean Copy of Replacement Pages. Specific amendments to the individual page of the specification are detailed in the following marked up page:

On page 9, please make the following changes.

input/output circuitry that is coupled to bit lines BL-1 through BL-M and complement bit lines BL-1* through BL-M* of array 110. Address buffer 114 also is coupled to control word line decoder 116. Word line decoder 116 and bit line decoder 118 selectably access memory cells 112-ij in response to address signals that are provided on address lines 120 from electronic system 101 during write and read operations.

In operation, memory 100 receives an address of a particular memory cell at address buffer 114. For example, electronic system 101 may provide address buffer 114 with the address for cell 112-11 of array 110. Address buffer 114 identifies word line WL-1 for memory cell 112-11 to word line decoder 116. Word line decoder 116 selectively activates word line WL-1 to activate access transistor 130-1j of each memory cell 112-1j that is connected to word line WL-1. Bit line decoder 118 selects bit line BL-1 for memory cell 112-11. For a write operation, data received by input/output circuitry is coupled to bit lines BL-1 through access transistor 130-11 to